SM2246EN Flash F/W & ISP Release Information – P1003B

Introduction
This purpose of this document is to provide release information on the SM2246EN F/W and ISP release information

Fix Coverage
■ stands for the **"new fix"** or **"new support"** in the category
□ stands for the **"no-update"** in the category

■ **Tester FW**	■ **Controller ISP**
□ **Yield Issue** ■ **Flash Issue** □ SLC Flash □ Samsung Flash □ Toshiba/Sandisk Flash □ Intel/Micron Flash □ Hynix Flash □ Others ■ MLC Flash ■ Samsung Flash ■ Toshiba/Sandisk Flash ■ Intel/Micron Flash ■ Hynix Flash □ **Compatibility issue** □ **Tester Bug Fix** ■ **AP Bug Fix & New Function** ■ **Feature Enhance**	■ **Yield Issue** ■ **Flash Issue** □ SLC Flash □ Samsung Flash □ Toshiba/Sandisk Flash □ Intel/Micron Flash □ Hynix Flash □ Others ■ MLC Flash ■ Samsung Flash ■ Toshiba/Sandisk Flash ■ Intel/Micron Flash ■ Hynix Flash □ **Compatibility issue** ■ **ISP Bug Fix** □ **Feature Enhance**

ISP Revision History

Version	MP Tool version	ISP version	Note
P1003B	**P1018B**	**P1003B**	**This FW supports both 2D/3D MLC NAND (no SLC caching)** **1. Update Security API** **2. Reduce time consumption on dram access in update/check map functions.** **3. Return COMRESET status in ISR if COMRESET occurs in Trim.** **4. Return previous one SAMRT data as latest WPRO page is UECC.** **5. Add pretest error code: 0x29 to sort power-on one pass L06B.** **6. Add max/min Temp. in SMART ID: 0xC2(optional setting in MP tool).** **7. Add flush dram as SPOR feature for 3.3V devices.** **8. Fix the issue that FW may not enable HW interrupt if power drops(VDT40 and VDT27) and recover then.** **9. Fix the issue that writing same data is seen as UNC during ATA command: SMART EXECUTE OFFLINE IMMEDIATE(0xD4).**
P0614D	P0628B	P0614D	This FW supports both 2D/3D MLC NAND (no SLC caching) 1. Update Security FW to SMI_SEC_SATA_P0701A. 2. Update RDT FW version to P0614RDT. 3. Update Boot ISP version to P0801A: For Intel L06B single plane read may cause ECC fail under a specific condition. 4. Add NAND sorting for SM3259. 5. Add Lower Page Protection (LPP) for I/M L06B 3.3V devices. 6. Pass WHCK-EHDD TPerReset test case on Windows 10. 7. Pass WHCK-EHDD RangeCrossing test case on Windows 10. 8. Abort FW Update operation, if the Security Settings don't remain the same. 9. Fix issue: CRYPTO SCRAMBLE EXT command can't be successfully implemented when only AES is enabled.
P0614B	P0624A	P0614B	1. This FW supports both 2D/3D MLC NAND 2. Enable "ODT by controller" for IM L06B 1TB drive. 3. Modify strong/weak page table #04. 4. Improve sequential read performance for 4-plane 16K-page devices. 5. Support new form factor: CFast. 6. Fix the issue of NCQ soft reset, where host could not send out FIS H2D.

			7. Fix the issue: During map saving, the last saved tail block should be empty block as its valid page count is 0. 8. Fix the issue: During getting page pointer of data block, command queue may hang under corner case as program fail handle is disabled. 9. Fix the issue: After moving WPRO block, meta data of plane 1 may be incorrect. 10. Add the mechanism that block 0 is included in check system block flow during pretest flow. 11. Fix the issue: Dummy pages of EOB may be filled with wrong serial.
O1225L	P0526A	O1225L	1. Support Mira dram (256MB/512MB) 2. Modify save map policy: limit partial save map time consumption 3. Modify issue of SSD cannot boot to Win8.1 when SATA Gen2 is forced 4. Add new pretest error code 0x26: Run time/RDT too much bad 5. Add backup page for erase unit info in WPRO block 6. Improve sequential read performance for 4-plane 16K-page flash (including Toshiba/SanDisk 15nm). 7. Modify strong/weak page table. 8. Fix NCQ soft reset issue, where host could not send out FIS H2D. 9. Fix issue of during the process of saving map, last saved tail block should be empty block as its valid page count is 0. 10. Fix issue of during the process of getting page ID of data block, command queue may hang under corner case as program fail handling is disabled. 11. Fix issue of after moving WPRO block, meta data of plane 1 may be incorrect.
O1225J	P0412B	O1225J	1. MP tool P0412B cannot swap ISP without being with ISP O1225J. Please don't use other version of ISP to be with MP tool P0412B to swap ISP. 2. 3D MLC is not supported by this FW 3. Modify features of thermal throttling. 4. Modify partial cleaning mechanism to avoid large time-consuming on loading EOB 5. Add an extra read method to handle NCQ read commands.
P0115G	P0223B	P0115G	1. Support Hynix 3D V2 MLC (SSD 128/256GB) 2. Support Micron L06B (SSD 128/256GB) 3. Support new seed table (1024 sets) 4. Extend table corresponding to physical page (strong page/weak page) to 2KB 5. Modify RDT for Micron L06B

			6. Fix the issue of loading code when the SSD is recovered from DEVSLP
O1225G	P0219B	O1225G	1. Modify that if “erase operation” was interrupted in the last power-on, return status to host and open HDRS interrupt before continuing doing erase operation. 2. Record LUN number in RDT test fail information and show in MP tool self test result. 3. Add an option, TotalFailCntTH, for the number of RDT Fail Threshold 4. Abort R/W commands when the address which would be accessed beyond the range can be supported by drive (case of over flow is detected) 5. Ram test flow is modified for higher coverage 6. Use “compared seed” to detect all 0xFF read data during read retry sequence 7. Modify read log extend command “Log address 04h-Device Statistics”, in which Logical Sectors Written/ Number of Write Commands/ Logical Sectors Read/ Number of Read Commands should be recorded in 48 bits 8. Modify the key management that each range has different key in the first place 9. Modify Program Fail Read Back Algorithm 10. Restore divided crystal frequency in shutdown process of DEVSLP function
O1225E	P0114A	O1225E	1. Doesn’t support AES/security related function. 2. Modify that if “erase operation” was interrupted in the last power-on, return status to host and open HDRS interrupt before continuing doing erase operation. 3. Record LUN number in RDT test fail information and show in MP tool self test result. 4. Add an option, TotalFailCntTH, for the number of RDT Fail Threshold 5. Abort R/W commands when the address which would be accessed beyond the range can be supported by drive (case of over flow is detected) 6. Ram test flow is modified for higher coverage 7. Use “compared seed” to detect all 0xFF read data during read retry sequence 8. Modify read log extend command “Log address 04h-Device Statistics”, in which Logical Sectors Written/ Number of Write Commands/ Logical Sectors Read/ Number of Read Commands should be recorded in 48 bits 9. Modify the key management that each range has different key in the first place 10. Modify Program Fail Read Back Algorithm
O1026A	O1027A	O1026A	1. Modify crystal frequency in order to avoid it’s too low to latch signals from SATA interface during the resume

			process. 2. Modify system PLL in case that the controller will encounter power-loss which is caused by sudden high peak frequency. 3. Modify the flow of SMART and security if UGSD occurs when doing “erase operation” 4. Add read back mechanism to check the authentication of program fail in RDT for SanDisk 1znm. 5. Add one mechanism to save event log
O0918B	O0910A	O0918B	1. Modify read retry sequence for Hynix 16nm B-Die 2. Add bitmap scrub operations for SanDisk 1znm 3. Support single 1GB DRAM (Vendor:Micron) 4. Fix the issue for power cycling during erase map info block
O0821D	O0819A	O0821D	1. Support SID Authority Disable Proposal – Microsoft 2. Support Mandatory GUDID Proposal - Microsoft 3. Support Geometry Reporting Feature – Alignment 4. For Hynix 20nm B die flash, fix the bug of flash ID changing after issuing “set feature”. 5. Fix ATA security bug when AES is disabled 6. Fix the issue of internal interleave
O0724B	O0722C	O0724B	1. Support Toshiba 24nm SLC 2. Support SanDisk 24nm MLC 3. Support SanDisk A19 (1Y) MLC 4. Modify program fail handling procedure 5. Support Toshiba 15nm SLC mode (A2 command) 6. Change Tper authentication to “Anybody authority” 7. Support IEEE 1667 CONFIGURE SILOS command
O0617A	O0618A	O0617A	1. This FW can support security and non-security FW that are corresponding to SM2246EN_AB and SM2246EN_AA. 2. MP will detect the controller automatically. If the controller is SM2246AA, MP will block security related functions. If the controller is SM2246AB, MP will show the options of security related functions. 3. Fix the issue related to read command access interface of TCG. 4. Make sure that the related hardware settings constrained

			to change AES keys are fully performed. 5. Fix the bug that when issuing. SMART_EXECUTE_OFFLINE_IMMEDIATE command which may cause the FW not be able to enter low-power mode. 6. Make sure that partial / slumber mode can be low-power. 7. Capacity of SSD would not be influenced when supporting TCG function.
N1126K	O0522A	N1126K	1. Modified SMART attribute reset: ID 0xA4~0xA7, 0xAF, 0xC7 and 0xF5 2. Returned status would include ● Pure spare count if the threshold is not exceeded ● Erase count if the threshold is exceeded 3. Fixed trim bug: when LBA of trim command is higher than total LBA, this command should be returned 4. Turn LED off when trim command is processed 5. Solved device sleep DRAM backup issue: flash retry FIFO should not be overlapped by DRAM data 6. Solved spare block run out issue: successive Map block can be used
N1126F	O0327A	N1126F	1. Fix overflow issue of read – retry table that Hynix NAND flash use. 2. Fix U-link NCQ-03 script issue 3. Support Sandisk 1znm flash. 4. Support Hynix 16nm F-die flash. 5. Add CID options for enabling DRAM SRT feature.
N1114H	N1114A	N1114H	1. Fix DEVSLP issue 2. Fix time-out issue of downloading microcode.
N1114B	N1114A	N1114B	1. Support 4Die/1CE Flash 2. Support new VU command for Serial Number change 3. Support disk self-destroy function (erase all disk data via GPIO) 4. Extend # of bad block combination to 2048 to improve 1TB initialization 5. Modify Pretest Bad Block Threshold as configurable from 0 to 255 6. Bug fix of Trim command and potential command timeout/abort. 7. Support Samsung K9QDGD8U5M
N1007C	N0918A	N1007C	1. Support TSB 15nm MLC. 2. Support of Sanitize (erase all block feature). 3. Improve command response time with background map

			rebuild. 4. Improve Macbook installation compatibility. 5. Improve Pretest flow in the cases of reference original and runtime bad. 6. Enhance error/event log structure and content. 7. Enable CDI interrupt iff DEVSLP had been configured and enabled by CID and host. 8. Resolve bugs/issues of NCQ read flow, Flash setting at DEVSLP resume, Trim command handling, program fail handling in swapping active block.
N0815B	N0815A	N0815B	1. Fix of program fail handling on pure SLC Flash. 2. Improvement to resolve read disturbance on Hynix 16nm MLC Flash. 3. Improvement to speed up boot time by storing WPRO page index information. 4. Bug fix of program fail. 5. Fix of SPOR timeout issue on 512GB/1TB disk. 6. Bug fix of LTS and RDT. 7. Bug fix of pretest failure on Samsung 21nm Flash. 8. Improvement of random read performance in internal interleave mode. 9. Support of full disk SLC mode on Micron Flash.
N0711A	N0704B	N0711A	1. Fix cache program bug since N0704A. 2. Fix program fail handle bug for internal interleave mode since N0704A 3. Fix an IPM issue since FW N0516D which automatically change Partial to Slumber in HIPM if DIPM was enabled. 4. Extend bad block combination number from 512 to 1024. 5. Decide Hynix read-retry count by using OPT command instead of predefine value from MP package. 6. Support Internal Interleave. 7. Support program fail handling 8. Modify trim flow for the performance with Marvell RAID chip 9. Support Hynix 16nm 64Gb MLC: H27QCG8T2E5R, H27QEG8VEE5R

			10. Support Hynix 16nm 128Gb MLC: H27QEG8UDB8R, H27QFG8VEB8R-BCF, H27Q1T8YEB9R (CS sample and after)
N0530C	N0529A	N0530C	1. ISP Bug fix: Erase count miss-match after doing security erase 2. Pretest Bug fix: Load L85A reclaim flash original bad bug found in N0530A 3. Fix an IPM issue since FWN0516D, which cannot enter IPM mode normally.
N0530A	N0529A	N0530A	1. Support auto partial to slumber in HIPM 2. Fill up the active block's valid pages word line when receiving Standby Immediately and swapping active block after power on 3. Save SMART attribute every 20 minutes 4. Save SMART info when receiving Standby Immediately 5. Fine tune a read cache judgment
N0402C	N0415A	N0402C	1. Support 4CH8WAY interleave for 512page/block flash (L85A/L95B) 2. Support 1TB capacity 3. Fix DEVSLP bugs 4. Support the entrance of device sleep without slumber mode first. (CID 0x4D.bit7) 5. Fix the bug of occasional ISP hangs-up if power off while security erase 6. Fix the bug of building the wrong mapping table after resuming from device sleep 7. RDT update: Show the wrong fail message at MP result window 8. Update L95B ECC to 60b in database
N0307A	N0307A	N0307A	1. Speed up boot up time by saving spare bitmap table, and shortening mapping table reset time. 2. Re-issue flash multi-plane ALE after disabling read-retry. 3. Issue one plane ALE instead of multi-plane in read-retry. 4. Extend the ALE, CLE and write pulse width when setting read-retry sequence in EDO mode.

			5. Enable hardware write protect.(GPIO p1.bit1) 6. Enable quick erase.(GPIO P1.bit5) 7. Fix the SMART value (attribute ID 0x05) miss-match issue 8. Fix a markbad bug. (N0227A issue from VCT) 9. Fix SMART info miss match issue. 10. Fix read and write log DMA extend command bug. 11. Fix RDT firmware cannot recognize MP vendor command issue. 12. Support 16k 4plane flash.
N0103B	N0114A	N0103B	1. Fix the bug of issuing Samsung 19nm read try command by EDO mode 2. Support DMA read log extend and DMA write log extend. 3. Support DMA read buffer and DMA write buffer. 4. Mark bad block by single block instead of super block and use rest good block to re-combine super block. 5. Support DMA download microcode 6. Add full dram size test in pretest
M1213C	M1226A	M1213C	1. Support Micron/Intel L85A, L84C, 2. Support Micron/Intel L95B 3. Support Samsung 19nm MLC 4. Fix seek & read verify sector command bug 5. Support PIO Multiple mode to 2 6. Fix SCT write same bug 7. Enhance SPOR protection 8. Write performance enhancement 9. Fix a FW bug of WHCK Trim test 10. Reduce DEVSLP power consumption 11. Fix a read try bug for Micron/Intel NAND 12. Support Download Micro Code
M1024C	M1024A	M1024C	1. Fix ATACT seek & read verify sector command bug. 2. Fix the error of scaling down the number of interleave

			3. Add QC tool functions
M1011A	M1009B	M1011A	1. Enhance ATA command support for Ulink test 2. Disable all flash CE if channel is idle. 3. Fix a power-cycling bug 4. Fix SN number issue when KeepSN is not 20 byte length.
M1003B	M1003A	M1003B	1. Fix IM20nm read retry bug and add more options for read retry. Issue flash reset command before retry sequence. 2. Fix build-link bug in 4ch8way 3. Fix SPOR function bugs 4. Disable dram compensation 5. Lower schmitt trigger windows) 6. Fix seek, read verify sector, and RW multiple command bug 7. Fix a wear leveling bug 8. Support Few Samsung & Hynix dram. 9. Support LTS and fix bugs of RDT function. Add the loop option in RDT 10. Add Micron20nm SLC read-retry table. 11. Add Dram 380Mhz option. 12. Enable write cache as a default. 13. Modify dram VDT from 1.4 to 1.3v.
M0808A	M0808B	M0808A	1. Fix Toshiba & Sandisk flash read-retry error. 2. Enhance SATA error handling 3. Switch to dummy write if the number of spare block decreases to zero, and do not mark bad block 4. Modify SMART command for WAF 5. Extend the number of write log page to 32 6. Fix strong page size bug on M0719 7. Fix pretest bug for manual toggle flash. 8. Add RDT function. 9. Don’t reset DRAM when resume
M0719A	M0716B	M0719A	1. Support Samsung 21nm K9GCG MLC

			2. Support Toshiba 19nm 16KB 2Plane MLC 3. Support Hynix H27QCGDT2BLR, H27QEGDVEBLR 4. Support Micron L84A Onfi MLC 5. Support Micron L85A Onfi MLC

Note:

1. F/W and ISP update is recommended.
2. History # is denoted by “Version-Date” .